

256K x 16 Static RAM

Features

- **Temperature Ranges**
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive-A: -40°C to 85°C
- **High speed**
 - $t_{AA} = 15 \text{ ns}$
- **Low active power**
 - 1540 mW (max.)
- **Low CMOS standby power (L version)**
 - 2.75 mW (max.)
- **2.0V Data Retention (400 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Available in Pb-free and non Pb-free 44-pin TSOP II and molded 44-pin (400-Mil) SOJ packages**

Functional Description

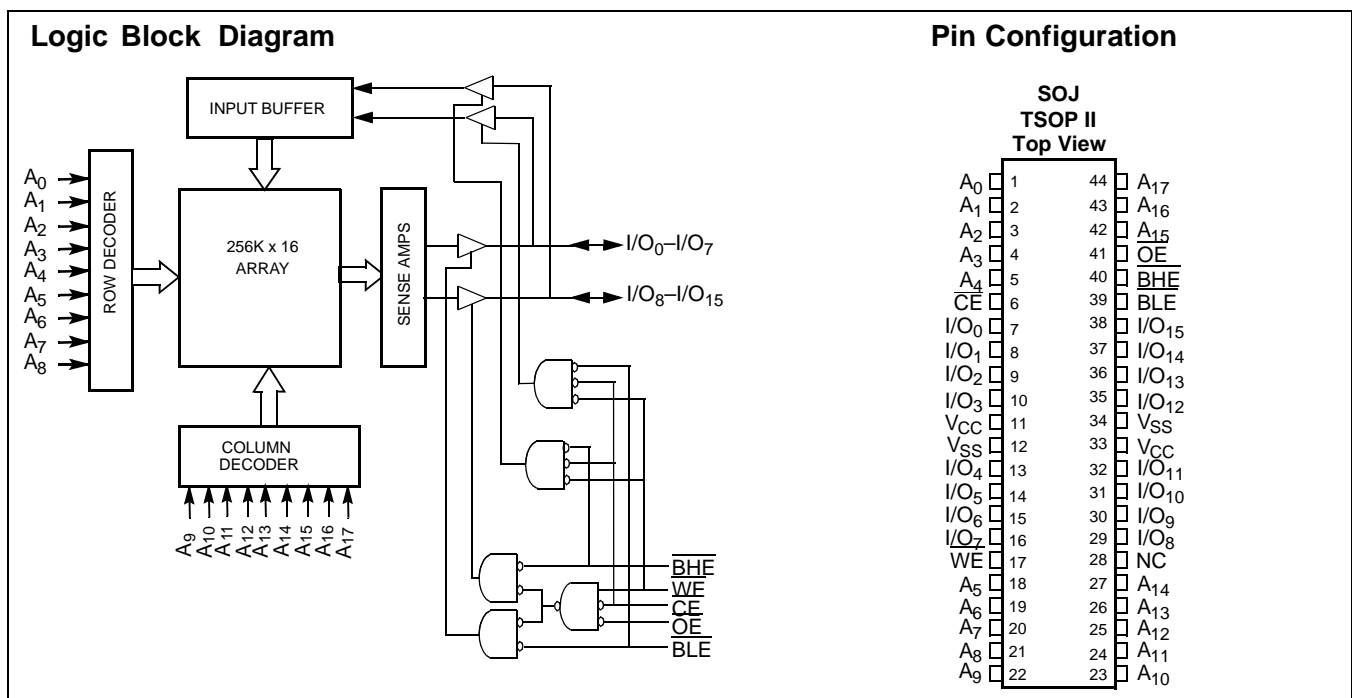
The CY7C1041BN is a high-performance CMOS static RAM organized as 262,144 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1041BN is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.



Selection Guide

		-15	-20	Unit
Maximum Access Time		15	20	ns
Maximum Operating Current	Commercial	190	170	mA
	Industrial	210	190	
	Automotive-A		190	
Maximum CMOS Standby Current	Commercial	3	3	mA
	Commercial L	0.5	0.5	
	Industrial	6	6	
	Automotive-A		6	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 0.5
Industrial	-40°C to +85°C	
Automotive-A	-40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-15		-20		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	mA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	Comm'l	190		170	mA
			Ind'l	210		190	mA
			Auto-A			190	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		40		40	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$	Comm'l	3		3	mA
			Comm'l L	0.5		0.5	mA
			Ind'l	6		6	mA
			Auto-A			6	mA

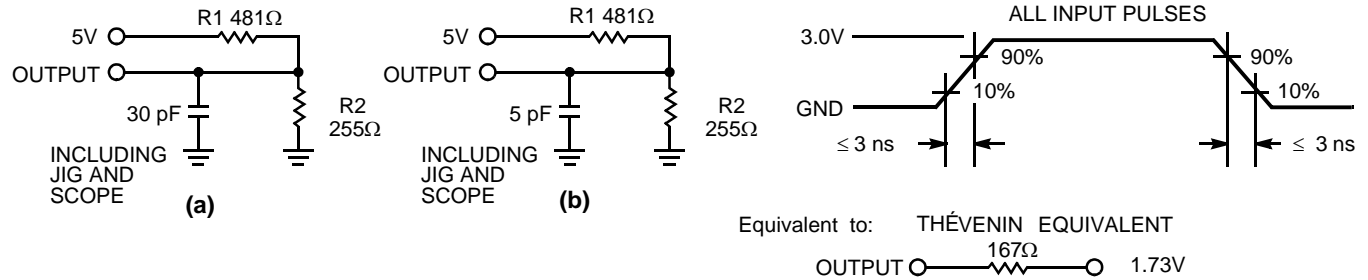
Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	I/O Capacitance		8	pF

AC Test Loads and Waveforms



Switching Characteristics^[4] Over the Operating Range

Parameter	Description	-15		-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{power}	V _{CC} (typical) to the First Access ^[5]	1		1		μs
t _{RC}	Read Cycle Time	15		20		ns
t _{AA}	Address to Data Valid		15		20	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		15		20	ns
t _{DOE}	\overline{OE} LOW to Data Valid		7		8	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		7		8	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		7		8	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		15		20	ns
t _{DBE}	Byte Enable to Data Valid		7		8	ns
t _{LZBE}	Byte Enable to Low Z	0		0		ns
t _{HZBE}	Byte Disable to High Z		7		8	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{power} time has to be provided initially before a read/write operation is started.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

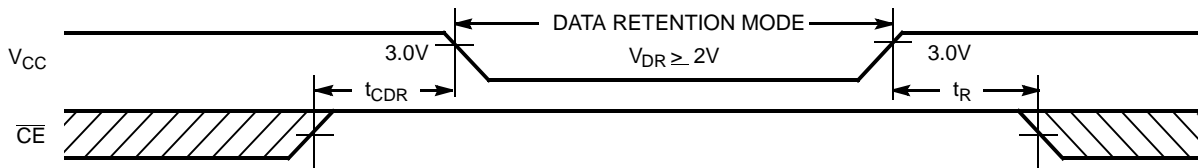
Switching Characteristics^[4] Over the Operating Range (continued)

Parameter	Description	-15		-20		Unit
		Min.	Max.	Min.	Max.	
Write Cycle^[8, 9]						
t_{WC}	Write Cycle Time	15		20		ns
t_{SCE}	\overline{CE} LOW to Write End	12		13		ns
t_{AW}	Address Set-Up to Write End	12		13		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	12		13		ns
t_{SD}	Data Set-Up to Write End	8		9		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		7		8	ns
t_{BW}	Byte Enable to End of Write	12		13		ns

Data Retention Characteristics Over the Operating Range (**L version only**)

Parameter	Description	Conditions ^[11]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[10]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

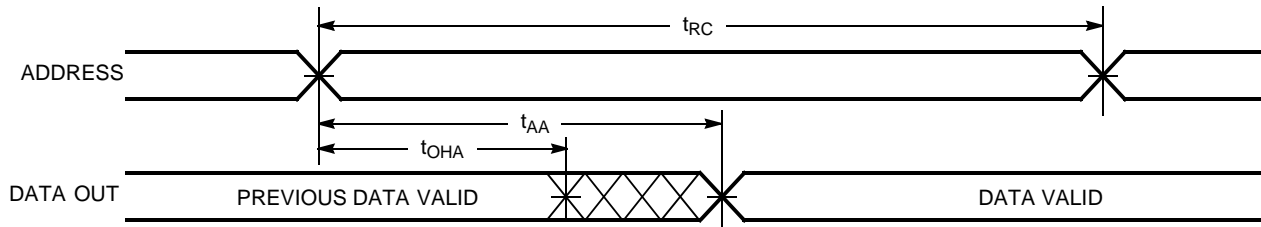


Notes:

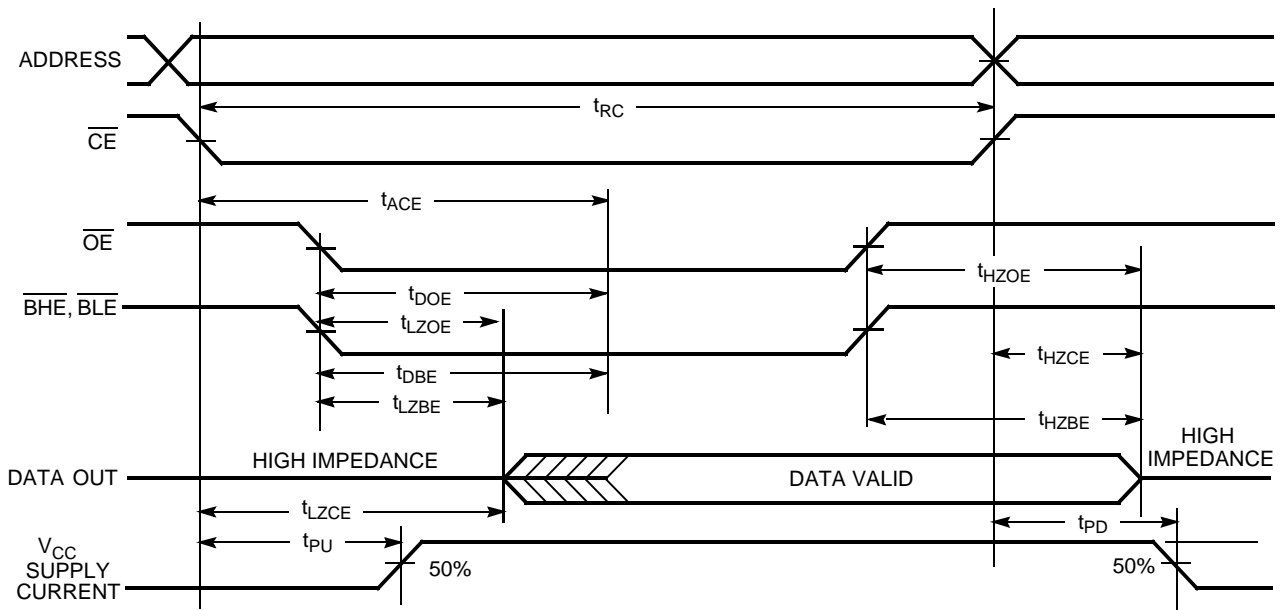
- 8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- 9. The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
- 10. $t_r \leq 3$ ns for the -15 speed. $t_r \leq 5$ ns for the -20 and slower speeds.
- 11. No input may exceed $V_{CC} + 0.5V$.

Switching Waveforms

Read Cycle No. 1^[12, 13]



Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]

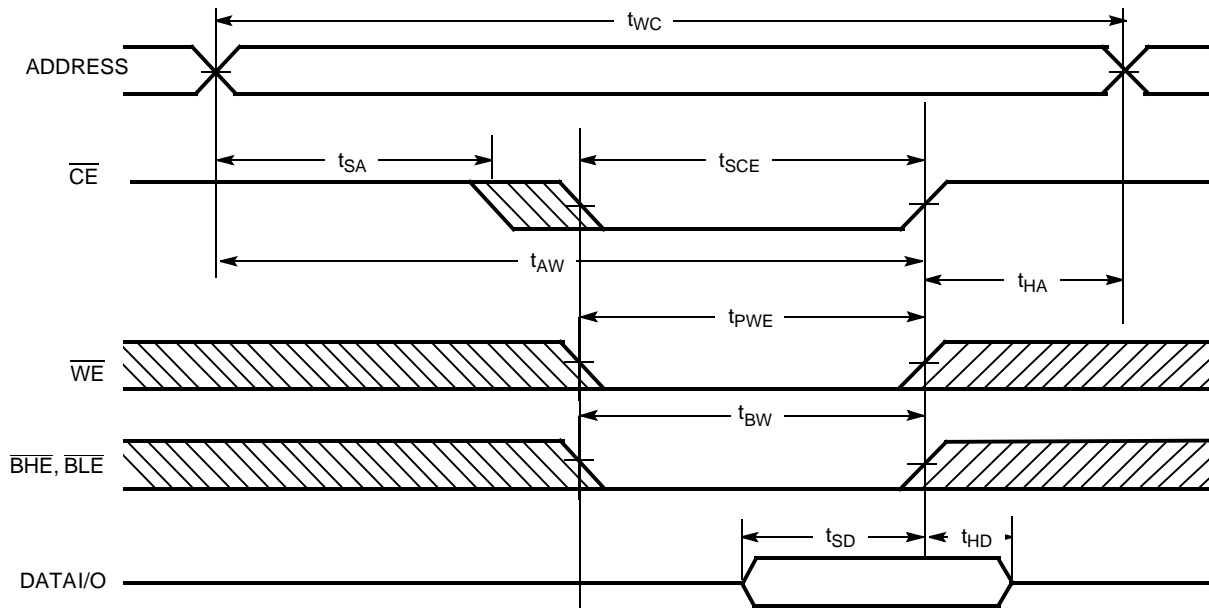


Notes:

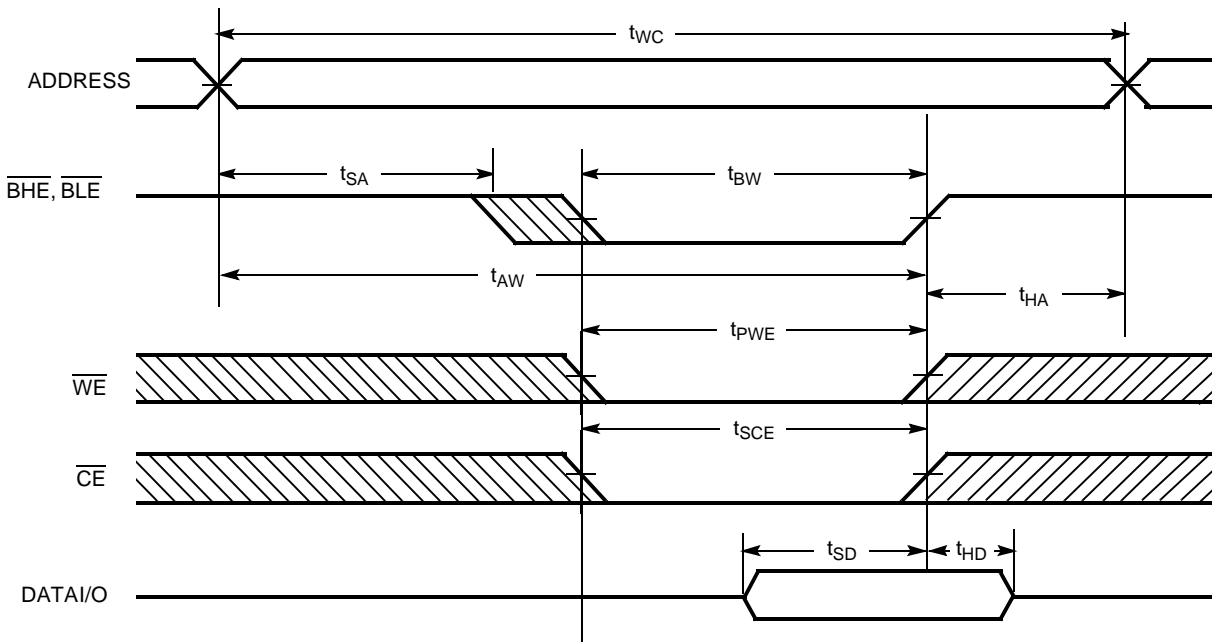
- 12. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} , and/or \overline{BLE} = V_{IL} .
- 13. \overline{WE} is HIGH for read cycle.
- 14. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16]



Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

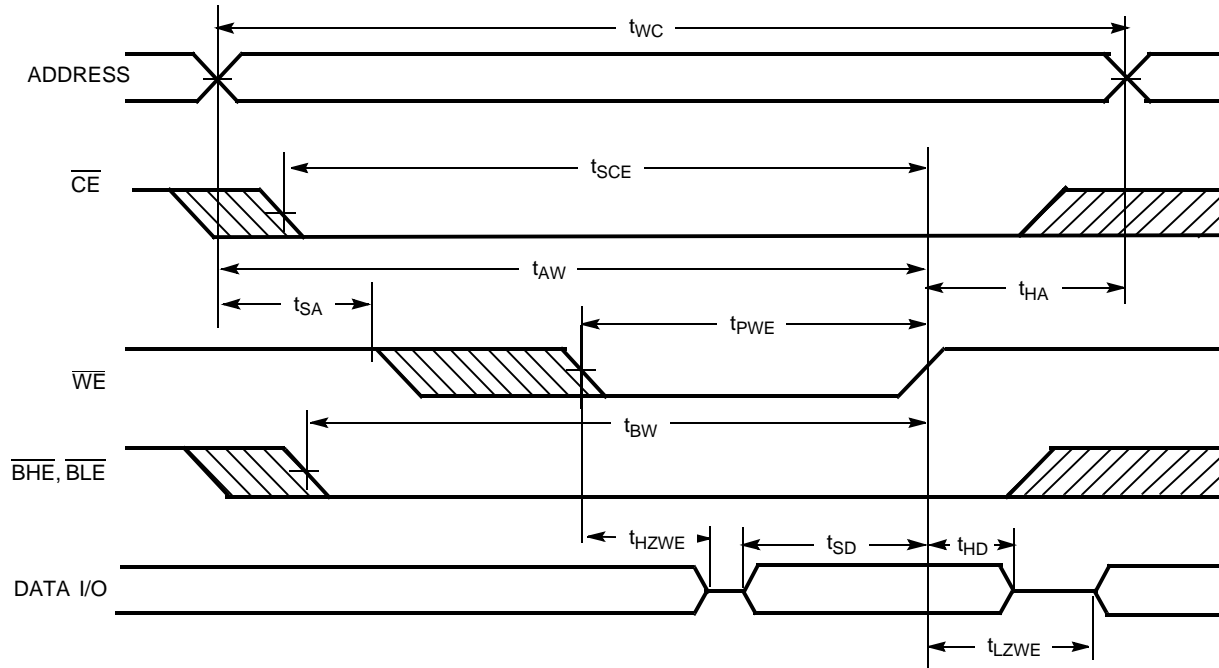


Notes:

- 15. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
- 16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)



Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

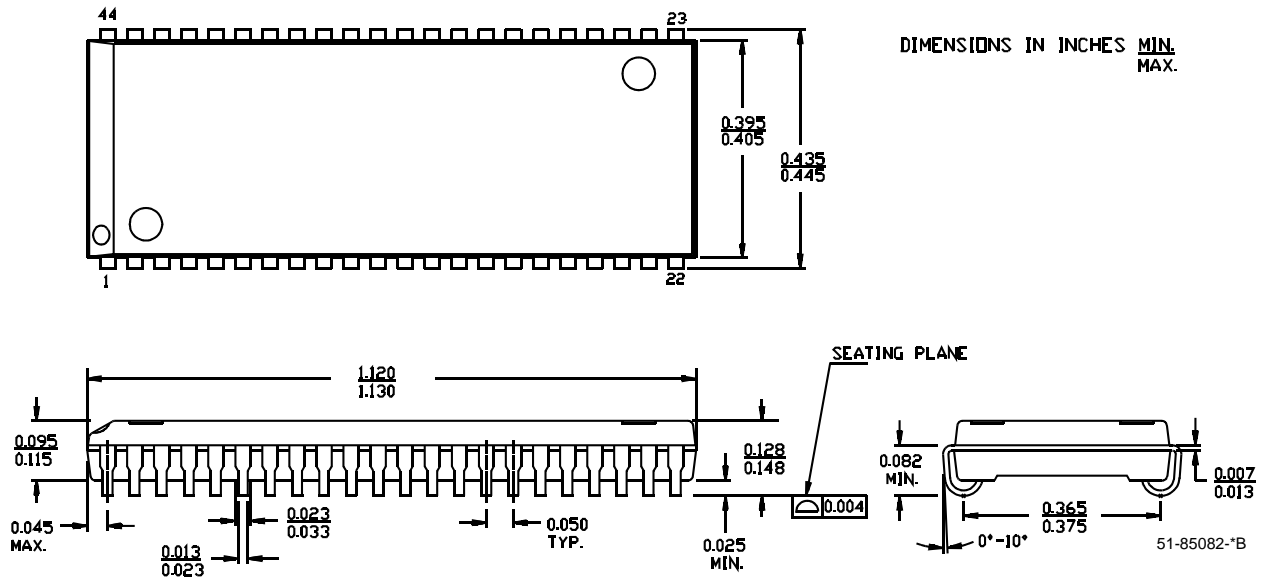
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range		
15	CY7C1041BN-15VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial		
	CY7C1041BN-15VXC		44-pin (400-Mil) Molded SOJ (Pb-free)			
	CY7C1041BN-15ZC	51-85087	44-pin TSOP Type II			
	CY7C1041BN-15ZXC		44-pin TSOP Type II (Pb-free)			
	CY7C1041BNL-15ZC		44-pin TSOP Type II			
	CY7C1041BNL-15ZXC		44-pin TSOP Type II (Pb-free)			
	CY7C1041BN-15ZI	51-85082	44-pin TSOP Type II		Industrial	
	CY7C1041BN-15ZXI		44-pin TSOP Type II (Pb-free)			
	20	CY7C1041BN-15VI	51-85082		44-pin (400-Mil) Molded SOJ	Commercial
		CY7C1041BN-15VXI			44-pin (400-Mil) Molded SOJ (Pb-free)	
CY7C1041BN-20VXC		51-85087	44-pin (400-Mil) Molded SOJ (Pb-free)			
CY7C1041BNL-20VXC			44-pin (400-Mil) Molded SOJ (Pb-free)			
CY7C1041BN-20ZC		51-85087	44-pin TSOP Type II	Industrial		
CY7C1041BN-20ZXC			44-pin TSOP Type II (Pb-free)			
CY7C1041BN-20ZI			44-pin TSOP Type II			
CY7C1041BN-20ZXI		51-85082	44-pin TSOP Type II (Pb-free)	Automotive-A		
CY7C1041BN-20ZSXA	44-pin TSOP Type II					

Please contact local sales representative regarding availability of these parts.

Package Diagrams

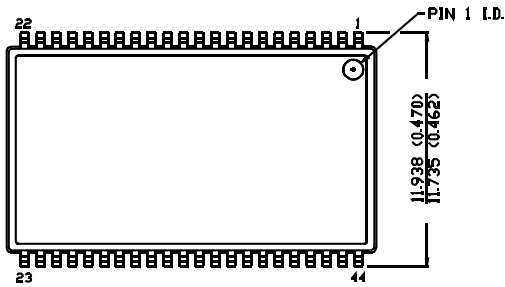
44-pin (400-Mil) Molded SOJ (51-85082)



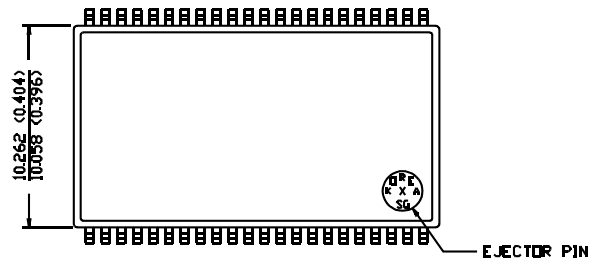
Package Diagrams (continued)

44-Pin TSOP II (51-85087)

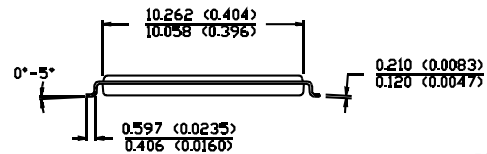
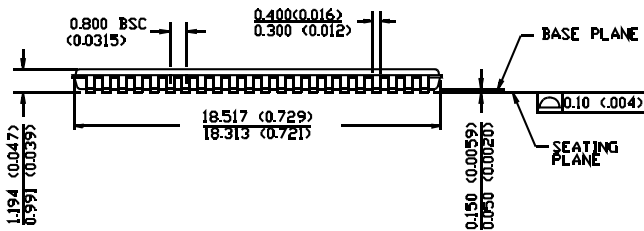
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-*A

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Document History Page

Document Title: CY7C1041BN 256K x 16 Static RAM				
Document Number: 001-06496				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	424111	See ECN	NXR	New Data Sheets
*A	498575	See ECN	NXR	Added Automotive-A operating range updated Ordering Information Table